

VLSI Floorplan Optimization Using Simulated Annealing

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Abstract: VLSI design is a process used to build electronic components such as microprocessors and memory chips comprising millions of transistors. VLSI design process is basically divided into number of phases. The first stage produces a set of indivisible rectangular blocks called cells. In a second stage, interconnection information is used to determine the relative placements of these cells. In the third stage, the goal of optimizing the total area is achieved using various techniques. This is the stage called Floorplan Optimization or Floorplanning which is considered in this paper using a metaheuristic technique Simulated Annealing. Floorplanning is an important part of the design process, since its area usually dominates the cost of a chip. This paper highlights the potential of a metaheuristic technique, Simulated Annealing to solve this optimization problem called VLSI Floorplanning.

Keywords: VLSI Design, Floorplanning, Simulated Annealing, Metaheuristics, Optimization Problem.

INTRODUCTION

Floorplanning is important in VLSI (Very Large Scale Integrated circuit) design automation. VLSI is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. The VLSI design automation is one of the most computational expensive and complicated processes with significant impact into computer chips manufacturing. The Floorplanning problem aims to arrange a set of rectangular modules on a rectangular chip area (Motherboard) so as to optimize an appropriate measure of performance. This problem is known to be NP-hard, and is particularly challenging if the chip dimensions are fixed.

FLOORPLAN PROBLEM

Given a set of blocks $B = \{b_1, b_2, \dots, b_n\}$. Each block b_i is rectangular and has fixed width and height. The objectives of Floorplan optimization problem are to minimize the area of B and reduce wire lengths of interconnects subject to the constraints that no pair of blocks overlaps. Floorplanning minimizes a specified cost metric such as a combination of the area A_{tot} and wire length W_{tot} induced by the assignment of b_i 's, where A_{tot} is measured by the final enclosing rectangle of P and W_{tot} the summation of half the bounding box of pins for each net.

$$\text{Cost} = \alpha * A_{tot} + \beta * W_{tot}$$

Where,

A_{tot} = Total area of the packing.

W_{tot} = Total wire length of packing.

α and β = User specified constant.

Floorplan Area

Floorplan Area (FA) is area of minimum possible of rectangle which accommodates n blocks b_1, b_2, \dots, b_n in non-overlapping manner. Clearly, $FA \geq MA$.

Dead Area

A minimum possible rectangle which can accommodate n blocks in non-overlapping manner has some area not occupied by any blocks. It is known as Dead Area (DA) and measured in percentage of FA, namely $DA = (FA - MA) / FA * 100$. Area utilization factor is defined to be $100 - DA$.

L-compact

A floorplan L-compact if and only if there is no block that can shift left from its original position with other components fixed.

B-compact

A floorplan is B-compact if and only if there is no block that can shift bottom from its original position with other components fixed.

LB-compact

A floorplan is LB-Compact if and only if it's both L-compact and B-compact. These types of floorplans are illustrated in the following figures.

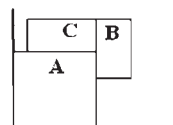


Fig. (a) A Floorplan

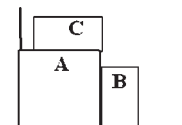


Fig. (b) B-Compact Floorplan

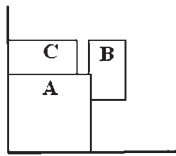


Fig. (c) L-Compact Floorplan

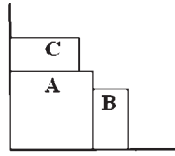


Fig. (d) LB-Compact Floorplan

FLOORPLAN DIVISIONS

Broadly, we can classify floorplans into two divisions: Slicing and Non Slicing Floorplans. Slicing Floorplan is defined as a module or floorplan that can be partitioned into two slicing floorplans with a horizontal or vertical cut line. A Non-slicing Floorplan is defined as a superset of slicing floorplans. It may contain the wheel shape in which vertical or horizontal cuts cannot be represented in Tree Format.

SLICING FLOORPLANS

1. Slicing Tree, Otten, DAC'82
2. Normalized Polish Expression, Wong and Liu, DAC'86

NON-SLICING FLOORPLANS

1. Sequence pair (SP): Murata, et al., ICCAD'95
2. Bounded-sliceline grid (BSG): Nakatake, et al., ICCAD'96
3. O-tree: (Guo, et al., DAC'99)
4. B*-tree: Chang, et al., DAC'2k
5. Corner block list (CBL): Hong, et al., ICCAD'2k
6. Transitive closure graph (TCG): Lin and Chang, DAC'01
7. TCG-S: Lin and Chang
8. Corner sequence (CS): Lin and Chang

OBJECTIVES OF VLSI FLOORPLANNING:

(a) To find the exact location of the cells to minimize area and wire-length. (b) To determine best shape of soft modules for optimized placement on board. (c) To minimize total wire length (d) Area utilization-Depends on how nicely the rigid modules shapes are matched.

SIMULATED ANNEALING – A METAHEURISTIC TECHNIQUE

Simulated Annealing is commonly said to be the oldest among the metaheuristics and surely one of the first algorithms that had an explicit strategy to avoid local minima. The fundamental idea is to allow moves resulting in solutions of worse quality than the current solution (uphill moves) in order to escape from local minima. The probability of doing such a move is decreased during the search.

The algorithm starts by generating an initial solution and by initializing the temperature parameter T . Then the following is repeated until the termination condition is

satisfied: A solution s' from the neighborhood $N(s)$ of the solution s is randomly sampled and it is accepted as new current solution depending on $f(s)$, $f(s')$ and T . s' replaces s if $f(s') < f(s)$ or, in case $f(s') \geq f(s)$, with a probability which is a function of T and $f(s') - f(s)$. The probability is generally computed following the Boltzmann distribution $\exp(-(f(s') - f(s))/T)$.

The temperature T is decreased during the search process, thus at the beginning of the search the probability of accepting uphill moves is high and it gradually decreases, converging to a simple iterative improvement algorithm. This process is analogous to the annealing process of metals and glass, which assume a low energy configuration when cooled with an appropriate cooling schedule. Regarding the search process, this means that the algorithm is the result of two combined strategies: random walk and iterative improvement. In the first phase of the search, the bias toward improvements is low and it permits the exploration of the search space; this erratic component is slowly decreased thus leading the search to converge to a (local) minimum. The probability of accepting uphill moves is controlled by two factors: the difference of the objective functions and the temperature. On the one hand, at fixed temperature, the higher the difference $f(s') - f(s)$, the lower the probability to accept a move from s to s' . On the other hand, the higher T , the higher the probability of uphill moves.

COMPONENTS IN SIMULATED ANNEALING

- Solution space (e.g., slicing Floorplans)
- Cost function (e.g., the area of a Floorplan)
 - Determines how “good” a particular solution is
- Perturbation rules
(Transforming a Floorplan to a new one)
- Simulated annealing engine
 - A Variable T , analogous to temperature
 - An Initial temperature T_0 (e.g., $T_0 = 40,000$)
 - A Freezing temperature T_{freeze} (e.g., $T_{\text{freeze}} = 0.1$)
 - A Cooling schedule (e.g., $T = 0.95 * T$)

REASON OF USING A METAHEURISTIC APPROACH

Metaheuristics are high-level procedures that coordinate simple heuristics such as local search, to find solutions that are of better quality than those found by simple heuristics done. Metaheuristics are generally applied to problems for which there are no satisfactory problem-specific algorithm or heuristic; or when it is not practical to implement such a method. Most commonly used metaheuristics are targeted to combinatorial optimization problems, but of course can handle any problem that can be recast in that form.

CONCLUSION

Floorplanning is a major area of research in VLSI design process as its area is directly associated with the cost of a

chip. The goal of VLSI Floorplanning is to optimize the total area of chip board. This type of NP Hard optimization problem can be solved using various heuristic methods but there are many complications and limitations. Therefore, metaheuristics should be used to get the good results. Simulated Annealing is an efficient metaheuristic technique to solve optimization problems and can give us very excellent results, if it is used in the VLSI design process as main algorithm.

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